

code	mnemonic		T	S Z AC P C	code	mnemonic		T	S Z AC P C	code	mnemonic		T	S Z AC P C
06	MVI B,n	move value to B	7T		78	MOV A,B	move B to A	5T		70	MOV M,B	store B to memory (HL)	7T	
0E	MVI C,n	move value to C	7T		79	MOV A,C	move C to A	5T		71	MOV M,C	store C to memory (HL)	7T	
16	MVI D,n	move value to D	7T		7A	MOV A,D	move D to A	5T		72	MOV M,D	store D to memory (HL)	7T	
1E	MVI E,n	move value to E	7T		7B	MOV A,E	move E to A	5T		73	MOV M,E	store E to memory (HL)	7T	
26	MVI H,n	move value to H	7T		7C	MOV A,H	move H to A	5T		74	MOV M,H	store H to memory (HL)	7T	
2E	MVI L,n	move value to L	7T		7D	MOV A,L	move L to A	5T		75	MOV M,L	store L to memory (HL)	7T	
36	MVI M,n	move value to memory (HL)	10T		7E	MOV A,M	move memory (HL) to A	7T		77	MOV M,A	store A to memory (HL)	7T	
3E	MVI A,n	move value to A	7T		7F	MOV A,A	move A to A	5T						
40	MOV B,B	move B to B	5T		50	MOV D,B	move B to D	5T		60	MOV H,B	move B to H	5T	
41	MOV B,C	move C to B	5T		51	MOV D,C	move C to D	5T		61	MOV H,C	move C to H	5T	
42	MOV B,D	move D to B	5T		52	MOV D,D	move D to D	5T		62	MOV H,D	move D to H	5T	
43	MOV B,E	move E to B	5T		53	MOV D,E	move E to D	5T		63	MOV H,E	move E to H	5T	
44	MOV B,H	move H to B	5T		54	MOV D,H	move H to D	5T		64	MOV H,H	move H to H	5T	
45	MOV B,L	move L to B	5T		55	MOV D,L	move L to D	5T		65	MOV H,L	move L to H	5T	
46	MOV B,M	move memory (HL) to B	7T		56	MOV D,M	move memory (HL) to D	7T		66	MOV H,M	move memory (HL) to H	7T	
47	MOV B,A	move A to B	5T		57	MOV D,A	move A to D	5T		67	MOV H,A	move A to H	5T	
48	MOV C,B	move B to C	5T		58	MOV E,B	move B to E	5T		68	MOV L,B	move B to L	5T	
49	MOV C,C	move C to C	5T		59	MOV E,C	move C to E	5T		69	MOV L,C	move C to L	5T	
4A	MOV C,D	move D to C	5T		5A	MOV E,D	move D to E	5T		6A	MOV L,D	move D to L	5T	
4B	MOV C,E	move E to C	5T		5B	MOV E,E	move E to E	5T		6B	MOV L,E	move E to L	5T	
4C	MOV C,H	move H to C	5T		5C	MOV E,H	move H to E	5T		6C	MOV L,H	move H to L	5T	
4D	MOV C,L	move L to C	5T		5D	MOV E,L	move L to E	5T		6D	MOV L,L	move L to L	5T	
4E	MOV C,M	move memory (HL) to C	7T		5E	MOV E,M	move memory (HL) to E	7T		6E	MOV L,M	move memory (HL) to L	7T	
4F	MOV C,A	move A to C	5T		5F	MOV E,A	move A to E	5T		6F	MOV L,A	move A to L	5T	
0A	LDAX B	load memory (BC) to A	7T		80	ADD B	add B to A	4T	x x x x x	88	ADC B	add B to A with carry	4T	x x x x x
1A	LDAX D	load memory (DE) to A	7T		81	ADD C	add C to A	4T	x x x x x	89	ADC C	add C to A with carry	4T	x x x x x
2A	LHLD nn	load memory (nn) to HL	16T		82	ADD D	add D to A	4T	x x x x x	8A	ADC D	add D to A with carry	4T	x x x x x
3A	LDA nn	load memory (nn) to A	13T		83	ADD E	add E to A	4T	x x x x x	8B	ADC E	add E to A with carry	4T	x x x x x
02	STAX B	store A to memory (BC)	7T		84	ADD H	add H to A	4T	x x x x x	8C	ADC H	add H to A with carry	4T	x x x x x
12	STAX D	store A to memory (DE)	7T		85	ADD L	add L to A	4T	x x x x x	8D	ADC L	add L to A with carry	4T	x x x x x
22	SHLD nn	store HL to memory (nn)	16T		86	ADD M	add memory (HL) to A	7T	x x x x x	8E	ADC M	add memory (HL) to A with carry	7T	x x x x x
32	STA nn	store A to memory (nn)	13T		87	ADD A	add A to A	4T	x x x x x	8F	ADC A	add A to A with carry	4T	x x x x x
					C6	ADI n	add value to A	7T	x x x x x	CE	ACI n	add value to A with carry	7T	x x x x x
01	LXI B,nn	load address to BC	10T		09	DAD B	add BC to HL	10T	x	C1	POP B	pop BC from stack	10T	
11	LXI D,nn	load address to DE	10T		19	DAD D	add DE to HL	10T	x	D1	POP D	pop DE from stack	10T	
21	LXI H,nn	load address to HL	10T		29	DAD H	add HL to HL	10T	x	E1	POP H	pop HL from stack	10T	
31	LXI SP,nn	load address to stack	10T		39	DAD SP	add stack pointer to HL	10T	x	F1	POP PSW	pop PSW (AF) from stack	10T	x x x x x
07	RLC	rotate A left	4T	x	27	DAA	decimal adjust	4T	x x x x x	C5	PUSH B	push BC to stack	11T	
0F	RRC	rotate A right	4T	x	2F	CMA	complement A	4T		D5	PUSH D	push DE to stack	11T	
17	RAL	rotate A left with carry	4T	x	37	STC	set carry flag	4T	1	E5	PUSH H	push HL to stack	11T	
1F	RAR	rotate A right with carry	4T	x	3F	CMC	complement carry flag	4T	x	F5	PUSH PSW	push PSW (AF) to stack	11T	
D3	OUT n	output A to port number	10T		E3	XTHL	exchange top address in stack with HL	18T		E9	PCHL	jump to address in HL	5T	
DB	IN n	input from port number to A	10T		EB	XCHG	exchange HL with DE	4T		F9	SPHL	load HL to stack pointer	5T	

code	mnemonic		T	S Z A C P C	code	mnemonic		T	S Z A C P C	code	mnemonic		T	S Z A C P C
04	INR B	<i>increment B</i>	5T	x x x x	05	DCR B	<i>decrement B</i>	5T	x x x x	03	INX B	<i>increment BC</i>	5T	
0C	INR C	<i>increment C</i>	5T	x x x x	0D	DCR C	<i>decrement C</i>	5T	x x x x	13	INX D	<i>increment DE</i>	5T	
14	INR D	<i>increment D</i>	5T	x x x x	15	DCR D	<i>decrement D</i>	5T	x x x x	23	INX H	<i>increment HL</i>	5T	
1C	INR E	<i>increment E</i>	5T	x x x x	1D	DCR E	<i>decrement E</i>	5T	x x x x	33	INX SP	<i>increment stack pointer</i>	5T	
24	INR H	<i>increment H</i>	5T	x x x x	25	DCR H	<i>decrement H</i>	5T	x x x x	0B	DCX B	<i>decrement BC</i>	5T	
2C	INR L	<i>increment L</i>	5T	x x x x	2D	DCR L	<i>decrement L</i>	5T	x x x x	1B	DCX D	<i>decrement DE</i>	5T	
34	INR M	<i>increment memory (HL)</i>	10T	x x x x	35	DCR M	<i>decrement memory (HL)</i>	10T	x x x x	2B	DCX H	<i>decrement HL</i>	5T	
3C	INR A	<i>increment A</i>	5T	x x x x	3D	DCR A	<i>decrement A</i>	5T	x x x x	3B	DCX SP	<i>decrement stack pointer</i>	5T	
A0	ANA B	<i>and A with B</i>	4T	x x x x 0	B0	ORA B	<i>or A with B</i>	4T	x x 0 x 0	A8	XRA B	<i>xor A with B</i>	4T	x x 0 x 0
A1	ANA C	<i>and A with C</i>	4T	x x x x 0	B1	ORA C	<i>or A with C</i>	4T	x x 0 x 0	A9	XRA C	<i>xor A with C</i>	4T	x x 0 x 0
A2	ANA D	<i>and A with D</i>	4T	x x x x 0	B2	ORA D	<i>or A with D</i>	4T	x x 0 x 0	AA	XRA D	<i>xor A with D</i>	4T	x x 0 x 0
A3	ANA E	<i>and A with E</i>	4T	x x x x 0	B3	ORA E	<i>or A with E</i>	4T	x x 0 x 0	AB	XRA E	<i>xor A with E</i>	4T	x x 0 x 0
A4	ANA H	<i>and A with H</i>	4T	x x x x 0	B4	ORA H	<i>or A with H</i>	4T	x x 0 x 0	AC	XRA H	<i>xor A with H</i>	4T	x x 0 x 0
A5	ANA L	<i>and A with L</i>	4T	x x x x 0	B5	ORA L	<i>or A with L</i>	4T	x x 0 x 0	AD	XRA L	<i>xor A with L</i>	4T	x x 0 x 0
A6	ANA M	<i>and A with memory (HL)</i>	7T	x x x x 0	B6	ORA M	<i>or A with memory (HL)</i>	7T	x x 0 x 0	AE	XRA M	<i>xor A with memory (HL)</i>	7T	x x 0 x 0
A7	ANA A	<i>and A with A</i>	4T	x x x x 0	B7	ORA A	<i>or A with A</i>	4T	x x 0 x 0	AF	XRA A	<i>xor A with A</i>	4T	x x 0 x 0
E6	ANI n	<i>and A with value</i>	7T	x x x x 0	F6	ORI n	<i>or A with value</i>	7T	x x 0 x 0	EE	XRI n	<i>xor A with value</i>	7T	x x 0 x 0
B8	CMP B	<i>compare A with B</i>	4T	x x x x x	90	SUB B	<i>subtract B from A</i>	4T	x x x x x	98	SBB B	<i>subtract B from A with carry</i>	4T	x x x x x
B9	CMP C	<i>compare A with C</i>	4T	x x x x x	91	SUB C	<i>subtract C from A</i>	4T	x x x x x	99	SBB C	<i>subtract C from A with carry</i>	4T	x x x x x
BA	CMP D	<i>compare A with D</i>	4T	x x x x x	92	SUB D	<i>subtract D from A</i>	4T	x x x x x	9A	SBB D	<i>subtract D from A with carry</i>	4T	x x x x x
BB	CMP E	<i>compare A with E</i>	4T	x x x x x	93	SUB E	<i>subtract E from A</i>	4T	x x x x x	9B	SBB E	<i>subtract E from A with carry</i>	4T	x x x x x
BC	CMP H	<i>compare A with H</i>	4T	x x x x x	94	SUB H	<i>subtract H from A</i>	4T	x x x x x	9C	SBB H	<i>subtract H from A with carry</i>	4T	x x x x x
BD	CMP L	<i>compare A with L</i>	4T	x x x x x	95	SUB L	<i>subtract L from A</i>	4T	x x x x x	9D	SBB L	<i>subtract L from A with carry</i>	4T	x x x x x
BE	CMP M	<i>compare A with memory (HL)</i>	7T	x x x x x	96	SUB M	<i>subtract memory (HL) from A</i>	7T	x x x x x	9E	SBB M	<i>subtract memory (HL) from A with carry</i>	7T	x x x x x
BF	CMP A	<i>compare A with A</i>	4T	x x x x x	97	SUB A	<i>subtract A from A</i>	4T	x x x x x	9F	SBB A	<i>subtract A from A with carry</i>	4T	x x x x x
FE	CPI n	<i>compare A with value</i>	7T	x x x x x	D6	SUI n	<i>subtract value from A</i>	7T	x x x x x	DE	SBI n	<i>subtract value from A with carry</i>	7T	x x x x x
C2	JNZ nn	<i>conditional jump (not zero flag)</i>	10T		C4	CNZ nn	<i>conditional call (not zero flag)</i>	11/17T		C0	RNZ	<i>conditional return (not zero flag)</i>	5/11T	
CA	JZ nn	<i>conditional jump (zero flag)</i>	10T		CC	CZ nn	<i>conditional call (zero flag)</i>	11/17T		C8	RZ	<i>conditional return (zero flag)</i>	5/11T	
D2	JNC nn	<i>conditional jump (not carry flag)</i>	10T		D4	CNC nn	<i>conditional call (not carry flag)</i>	11/17T		D0	RNC	<i>conditional return (not carry flag)</i>	5/11T	
DA	JC nn	<i>conditional jump (carry flag)</i>	10T		DC	CC nn	<i>conditional call (carry flag)</i>	11/17T		D8	RC	<i>conditional return (carry flag)</i>	5/11T	
E2	JPO nn	<i>conditional jump (parity odd flag)</i>	10T		E4	CPO nn	<i>conditional call (parity odd flag)</i>	11/17T		E0	RPO	<i>conditional return (parity odd flag)</i>	5/11T	
EA	JPE nn	<i>conditional jump (parity even flag)</i>	10T		EC	CPE nn	<i>conditional call (parity even flag)</i>	11/17T		E8	RPE	<i>conditional return (parity even flag)</i>	5/11T	
F2	JP nn	<i>conditional jump (positive flag)</i>	10T		F4	CP nn	<i>conditional call (positive flag)</i>	11/17T		F0	RP	<i>conditional return (positive flag)</i>	5/11T	
FA	JM nn	<i>conditional jump (minus flag)</i>	10T		FC	CM nn	<i>conditional call (minus flag)</i>	11/17T		F8	RM	<i>conditional return (minus flag)</i>	5/11T	
C3	JMP nn	<i>jump to direct address</i>	10T		CD	CALL nn	<i>call to direct address</i>	17T		C9	RET	<i>return</i>	10T	
00	NOP	<i>no operation</i>	4T							C7	RST 0	<i>restart to 0000h</i>	11T	
76	HLT	<i>halt</i>								CF	RST 1	<i>restart to 0008h</i>	11T	
F3	DI	<i>disable interrupt</i>	4T							D7	RST 2	<i>restart to 0010h</i>	11T	
FB	EI	<i>enable interrupt</i>	4T							DF	RST 3	<i>restart to 0018h</i>	11T	
										E7	RST 4	<i>restart to 0020h</i>	11T	
										EF	RST 5	<i>restart to 0028h</i>	11T	
										F7	RST 6	<i>restart to 0030h</i>	11T	
										FF	RST 7	<i>restart to 0038h</i>	11T	